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REMARKS

Claims 1-4, as amended, remain herein.

The specification, page 12, line 2, has been amended to replace the number "267" with "257," consistent with Fig. 2.

Claims 1-4 have been amended for clarity, and the second subparagraph of claims 1-4 has also been amended to recite:

simultaneously detecting any stuck-at failures in the logical circuit and obtaining input logical values from the logical circuit such that extracted data representing one of the adjacent lines has a logical value "1" while extracted data representing the other of the adjacent lines has a logical value "0"

See specification at page 10, paragraphs 1-3, describing a change in the output of the logical circuit when the combination of selected lines includes a short circuit failure, i.e simultaneous detection of a short circuit between adjacent lines as part of the method for detecting stuck-at failures.

1. Claims 1-4 were rejected under 35 U.S.C. §103(a) over Endoh et al. U.S. Patent 5,485,094 and Ferguson et al. U.S. Patent 6,202,181, and claims 1-4 also were rejected under 35

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U.S.C. §103(a) over Endoh '094 and Parker et al. U.S. Patent 5,513,188.

The presently claimed semiconductor inspection method simultaneously detects a short circuit between adjacent lines as part of the method for detecting stuck-at failures (a node in the circuit is assumed to be unable to change its logic value), whereas prior art methods detect short circuits and stuck-at failures in separate methodologies.

The presently claimed inspection method comprises counting input logical values, such that one of the adjacent lines has a logical value "1", while the other has a logical value "0", simultaneously with detection of stuck-at failures. This method is nowhere disclosed or suggested in any of the cited references.

The Office Action also cites Endoh '094, Fig. 1, as allegedly disclosing a method for detecting short circuit failures between device lines, obtaining input logical values such that one of the adjacent lines has a logical value "1" while the other has a logical value "0", monitoring an output of

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a logical circuit that receives the input logical values, and comparing the monitored output with an output logical value that is expected when the input logical values are input to the logical circuit, as shown in Endoh '094, Figs. 3 and 35.

The Office Action also cites Ferguson '181, column 10, lines 17-24, as allegedly extracting adjacent lines wherein a short circuit may occur therebetween, and extracting lines having a distance therebetween that is equal to or less than a threshold as a distance between adjacent lines.

The Office Action cites Parker '188, for allegedly disclosing extracting adjacent lines that may have a short circuit occurring therebetween, and extracting lines having a distance therebetween that is equal to or less than a threshold as a distance between adjacent lines.

However, none of Endoh '094, Ferguson '181 or Parker '188 discloses simultaneously detecting stuck-at failures in the logical circuit and obtaining input logical values from the logical circuit such that extracted data representing one of the adjacent lines has a logical value "1" while extracted data

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representing the other of the adjacent lines has a logical value "0", as recited in applicant's claims 1-4. Thus, the presently claimed invention includes counting input logical values such that one of the adjacent lines has a logical value "1" while the other has a logical value "0," simultaneously with detection of stuck-at failures.

For the foregoing reasons, none of Endoh '094, Ferguson '181 or Parker '188 contains any teaching, suggestion, reason, motivation or incentive that would have led one of ordinary skill in the art to applicant's claimed invention. Nor is there any disclosure or teaching in any of these references that would have suggested the desirability of combining any portions thereof effectively to anticipate or suggest applicant's presently claimed invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

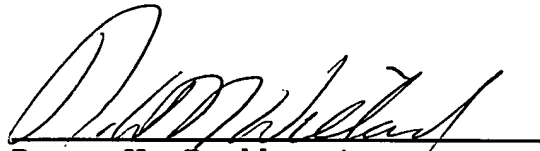
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All claims 1-4 are now proper in form and patentably distinguished over all grounds of rejection cited in the Office Action. Accordingly, allowance of all claims 1-4 is respectfully requested.

Should the Examiner deem that any further action by the applicant would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicant's undersigned representatives.

Respectfully submitted,

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